

DAN CLEIN

CMOS IC LAYOUT

Concepts, Methodologies, and Tools



Gregg Shimokura, Technical Contributor

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Dan Klein



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CMOS IC Layout Dan Clein, 2000 CMOS IC Layout presents not only the basics and theory of IC layout and design but also useful step by step procedures to make every circuit designer's job easier and more productive CMOS IC Layout offers skill training based on the author's working experience and gives new written procedures and guidelines **BOOK JACKET**

CMOS IC Layout Dan Clein, 1999-01-07 This book includes basic methodologies review of basic electrical rules and how they apply design rules IC planning detailed checklists for design review specific layout design flows specialized block design interconnect design and also additional information on design limitations due to production requirements Practical hands on approach to CMOS layout theory and design Offers engineers and technicians the training materials they need to stay current in circuit design technology Covers manufacturing processes and their effect on layout and design decisions

CMOS R. Jacob Baker, 2019-06-19 A revised guide to the theory and implementation of CMOS analog and digital IC design The fourth edition of CMOS Circuit Design Layout and Simulation is an updated guide to the practical design of both analog and digital integrated circuits The author a noted expert on the topic offers a contemporary review of a wide range of analog digital circuit blocks including phase locked loops delta sigma sensing circuits voltage current references op amps the design of data converters and switching power supplies CMOS includes discussions that detail the trade offs and considerations when designing at the transistor level The companion website contains numerous examples for many computer aided design CAD tools Using the website enables readers to recreate modify or simulate the design examples presented throughout the book In addition the author includes hundreds of end of chapter problems to enhance understanding of the content presented This newly revised edition Provides in depth coverage of both analog and digital transistor level design techniques Discusses the design of phase and delay locked loops mixed signal circuits data converters and circuit noise Explores real world process parameters design rules and layout examples Contains a new chapter on Power Electronics Written for students in electrical and computer engineering and professionals in the field the fourth edition of CMOS Circuit Design Layout and Simulation is a practical guide to understanding analog and digital transistor level design theory and techniques Circuit and Layout Techniques for Soft-error-resilient Digital CMOS Circuits Hsiao-Heng Kelin Lee, 2011 Radiation induced soft errors are a major concern for modern digital circuits especially memory elements Unlike large Random Access Memories that can be protected using error correcting codes and bit interleaving soft error protection of sequential elements i.e. latches and flip flops is challenging Traditional techniques for designing soft error resilient sequential elements generally address single node errors or Single Event Upsets SEUs However with technology scaling the charge deposited by a single particle strike can be simultaneously collected and shared by multiple circuit nodes resulting in Single Event Multiple Upsets SEMUs In this work we target SEMUs by presenting a design framework for soft error resilient sequential cell design with an overview of existing circuit and layout techniques for soft error mitigation and introducing a

new soft error resilience layout design principle called LEAP or Layout Design through Error Aware Transistor Positioning We then discuss our application of LEAP to the SEU immune Dual Interlocked Storage Cell DICE by implementing a new sequential element layout called LEAP DICE retaining the original DICE circuit topology We compare the soft error performance of SEU immune flip flops with the LEAP DICE flip flop using a test chip in 180nm CMOS under 200 MeV proton radiation and conclude that 1 our LEAP DICE flip flop encounters on average 2 000X and 5X fewer errors compared to a conventional D flip flop and our reference DICE flip flop respectively 2 our LEAP DICE flip flop has the best soft error performance among all existing SEU immune flip flops 3 In the evaluation of our design framework we also discovered new soft error effects related to operating conditions such as voltage scaling clock frequency setting and radiation dose

The Arts of VLSI Circuit Design - Symmetry Approaches toward Zero PVT Sensitivity Hongjiang Song,2018-02-26 This is one of a book in a VLSI circuit design book series Dr Hongjiang Song published under the VLSI signal processing circuit techniques This text covers various state of the arts circuit design techniques based on VLSI symmetry principles These methods offer inherently low PVT sensitivity for VLSI analog circuit design with superior scalability and performance

The Arts of VLSI Circuit Design Hongjiang Song,2011-03-02 This text is based on the class notes of a VLSI signal processing circuit course series EEE598 the author developed for the EE department at Arizona State University The materials are organized into nineteen special topics covering various state of the arts symmetry based VLSI circuit design techniques for basic VLSI circuit elements circuit modules and systems where the symmetry principle and methods with inherently low PVT sensitivity are used to design VLSI circuits with superior scalability and performance for various VLSI SOC applications

Regular Fabrics in Deep Sub-Micron Integrated-Circuit Design Fan Mo,Robert K. Brayton,2007-05-08 Regular Fabrics in Deep Sub Micron Integrated Circuit Design discusses new approaches to better timing closure and manufacturability of DSM Integrated Circuits The key idea presented is the use of regular circuit and interconnect structures such that area delay can be predicted with high accuracy The co design of structures and algorithms allows great opportunities for achieving better final results thus closing the gap between IC and CAD designers The regularities also provide simpler and possibly better manufacturability In this book we present not only algorithms for solving particular sub problems but also systematic ways of organizing different algorithms in a flow to solve the design problem as a whole A timing driven chip design flow is developed based on the new structures and their design algorithms which produces faster chips in a shorter time

Low Power RF Circuit Design in Standard CMOS Technology Unai Alvarado,Guillermo Bistué,Iñigo Adín,2011-10-18 Low Power Consumption is one of the critical issues in the performance of small battery powered handheld devices Mobile terminals feature an ever increasing number of wireless communication alternatives including GPS Bluetooth GSM 3G WiFi or DVB H Considering that the total power available for each terminal is limited by the relatively slow increase in battery performance expected in the near future the need for efficient circuits is now critical

This book presents the basic techniques available to design low power RF CMOS analogue circuits. It gives circuit designers a complete guide of alternatives to optimize power consumption and explains the application of these rules in the most common RF building blocks LNA mixers and PLLs. It is set out using practical examples and offers a unique perspective as it targets designers working within the standard CMOS process and all the limitations inherent in these technologies.

Semiconductors Artur Balasinski, 2018-09-03 Because of the continuous evolution of integrated circuit manufacturing ICM and design for manufacturability DfM most books on the subject are obsolete before they even go to press. That's why the field requires a reference that takes the focus off of numbers and concentrates more on larger economic concepts than on technical details. *Semiconductors Integrated Circuit Design for Manufacturability* covers the gradual evolution of integrated circuit design ICD as a basis to propose strategies for improving return on investment ROI for ICD in manufacturing. Where most books put the spotlight on detailed engineering enhancements and their implications for device functionality in contrast this one offers among other things crucial valuable historical background and roadmapping all illustrated with examples. Presents actual test cases that illustrate product challenges examine possible solution strategies and demonstrate how to select and implement the right one. This book shows that DfM is a powerful generic engineering concept with potential extending beyond its usual application in automated layout enhancements centered on proximity correction and pattern density. This material explores the concept of ICD for production by breaking down its major steps product definition design layout and manufacturing. Averting extended discussion of technology techniques or specific device dimensions the author also avoids the clumsy chapter architecture that can hinder other books on this subject. The result is an extremely functional systematic presentation that simplifies existing approaches to DfM outlining a clear set of criteria to help readers assess reliability functionality and yield. With careful consideration of the economic and technical trade offs involved in ICD for manufacturing this reference addresses techniques for physical electrical and logical design keeping coverage fresh and concise for the designers manufacturers and researchers defining product architecture and research programs.

Subsampling GPS Receiver Front-end Carsten Barth, 2011 Research in RFIC design has recently shifted towards direct conversion and subsampling architectures as an alternative to the conventional super heterodyne architectures. Bandpass sampling architectures also called subsampling architectures exhibit several advantages over super heterodyne architectures notably the complexity of subsampling architectures is significantly lower since no phase locked loop is required. A direct consequence is that downconversion from RF to IF can be achieved with significant power savings as compared to the super heterodyne architecture. Another significant benefit of such architectures is the capability for processing multiple signals in parallel. The ability to simultaneously handle multiple carriers makes subsampling architectures particularly well suited for GNSS applications as downconversion of multiple frequency bands is required in GNSS environments. With the advent of the new civilian GPS signals L2C and L5 and the onset of the new Galileo signal a receiver that can process multiple signals

without adding complexity is highly desired. An integrated proof of concept subsampling GPS receiver front end in 130 nm BiCMOS is presented in this dissertation. The receiver achieves a noise figure of less than 3.8 dB, the lowest ever recorded noise figure of a subsampling based receiver.

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