

Encounter manual

Guangyi CAO

Cadence Encounter is a software for placement and routing of synthesized vhdl (verilog) code.

To start with Encounter in linux, type **Encounter** in your home directory, then Encounter graphic user interface displays.

Create a folder, for example, **neededfile**, and put all needed files in it.

Necessary files should include:

1. A synthesized verilog file, like `fpu_sin.v`, or your own design.
2. Timing libraries, we use `typical_conditional_ccsm.lib`
3. lef file, `free2008_10_sp1.lef`
- 4 a clock tree file, `clock.ctstch`.

Import design

In encounter GUI, click design->import design, the following frame comes out, input all needed information like this. Please notice for top cell, you can choose Auto Assign.

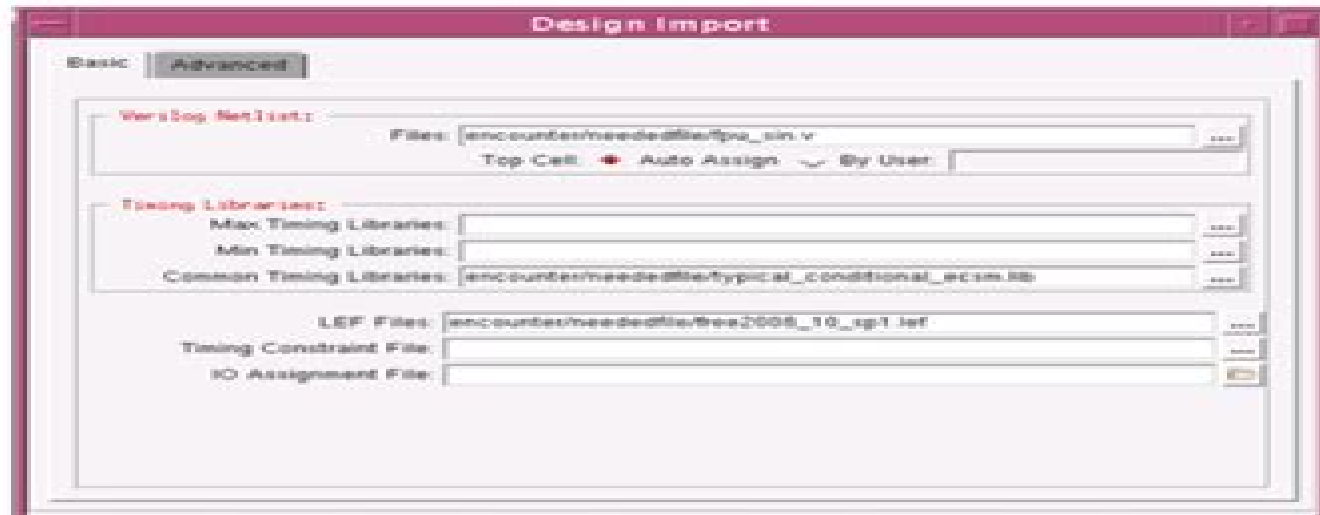


Figure 1

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**Francky Catthoor, Praveen
Raghavan, Andy Lambrechts, Murali
Jayapala, Angeliki Kritikakou, Javed
Absar**

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Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits Sandeep K. Goel, Krishnendu Chakrabarty, 2017-12-19 Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits ICs. However, the increased complexity and nanometer size features of modern ICs make them susceptible to manufacturing defects as well as performance and quality issues. Testing for Small Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens, bridges, and design for manufacturing DfM related rule violations. The book also addresses testing for small delay defects SDDs which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing including basic concepts and introductory material. Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics. Reviews SDD testing based on alternative methods that explore new metrics, top off ATPG and circuit topology based solutions. Highlights the advantages and disadvantages of a diverse set of metrics and identifies scope for improvement. Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.

Electromigration Inside Logic Cells Gracieli Posser, Sachin S. Sapatnekar, Ricardo Reis, 2016-11-26 This book describes new and effective methodologies for modeling, analyzing, and mitigating cell internal signal electromigration in nanoCMOS with significant circuit lifetime improvements and no impact on performance, area, and power. The authors are the first to analyze and propose a solution for the electromigration effects inside logic cells of a circuit. They show in this book that an interconnect inside a cell can fail, reducing considerably the circuit lifetime, and they demonstrate a methodology to optimize the lifetime of circuits by placing the output Vdd and Vss pin of the cells in the less critical regions where the electromigration effects are reduced. Readers will be enabled to apply this methodology only for the critical cells in the circuit, avoiding impact in the circuit delay, area, and performance, thus increasing the lifetime of the circuit without loss in other characteristics.

Nanometer Technology Designs Nisar Ahmed, 2010-02-26 Adopting new fabrication technologies not only provides higher integration and enhances performance but also increases the types of manufacturing defects. With design size in millions of gates and working frequency in GHz, timing-related defects have become a high proportion of the total chip defects. For nanometer technology designs, the stuck-at-fault test alone cannot ensure a high quality level of chips. At speed tests, using the transition fault model has become a requirement in technologies below 180nm. Traditional at-speed test methods cannot guarantee high quality test results as they face many new challenges: supply noise, including IR drop, ground bounce, and Ldi/dt effects on chip performance; high test pattern volume; low fault defect coverage; small delay defect

test pattern generation high cost of test implementation and application and utilizing low cost testers are among these challenges This book discusses these challenges in detail and proposes new techniques and methodologies to improve the overall quality of the transition fault test

Closing the Gap Between ASIC & Custom David Chinnery, Kurt William Keutzer, 2002 This book carefully details design tools and techniques for high performance ASIC design Using these techniques the performance of ASIC designs can be improved by two to three times Important topics include Improving performance through microarchitecture Timing driven floorplanning Controlling and exploiting clock skew High performance latch based design in an ASIC methodology Automatically identifying and synthesizing complex logic gates Automated cell sizing to increase performance and reduce power Controlling process variation These techniques are illustrated by designs running two to three times the speed of typical ASICs in the same process generation

Test and Diagnosis for Small-Delay Defects Mohammad Tehranipoor, Ke Peng, Krishnendu Chakrabarty, 2011-09-08 This book will introduce new techniques for detecting and diagnosing small delay defects in integrated circuits Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small delay defects including important parameters such as process variations crosstalk and power supply noise

Introduction to Low-Power Design in VLSIs Patrick Lee, 2011-12-12 This book discusses one increasingly important issue in the VLSI design low power It covers the following topics a basic concepts of low power design b low power design methods and applications in industry chips and c commercial CAD tools on low power design This book discusses the concepts a set of known methods industry cases and CAD tools on the low power design It is organized in four chapters and a glossary is provided at the end of the book

Design and Process Integration for Microelectronic Manufacturing, 2005

High Performance Embedded Architectures and Compilers Per Stenström, Michel Dubois, Manolis Katevenis, Rajiv Gupta, Theo Ungerer, 2008-01-15 This highly relevant and up to the minute book constitutes the refereed proceedings of the Third International Conference on High Performance Embedded Architectures and Compilers HiPEAC 2008 held in Göteborg Sweden January 27-29 2008 The 25 revised full papers presented together with 1 invited keynote paper were carefully reviewed and selected from 77 submissions The papers are organized into topical sections on a number of key subjects in the field

Ultra-Low Energy Domain-Specific Instruction-Set Processors Francky Catthoor, Praveen Raghavan, Andy Lambrechts, Murali Jayapala, Angeliki Kritikakou, Javed Absar, 2010-08-05 Modern consumers carry many electronic devices like a mobile phone digital camera GPS PDA and an MP3 player The functionality of each of these devices has gone through an important evolution over recent years with a steep increase in both the number of features as in the quality of the services that they provide However providing the required compute power to support an uncompromised combination of all this functionality is highly non trivial Designing processors that meet the demanding requirements of future mobile devices requires the optimization of the embedded system in general

and of the embedded processors in particular as they should strike the correct balance between flexibility energy efficiency and performance In general a designer will try to minimize the energy consumption as far as needed for a given performance with a sufficient flexibility However achieving this goal is already complex when looking at the processor in isolation but in reality the processor is a single component in a more complex system In order to design such complex system successfully critical decisions during the design of each individual component should take into account effect on the other parts with a clear goal to move to a global Pareto optimum in the complete multi dimensional exploration space In the complex global design of battery operated embedded systems the focus of Ultra Low Energy Domain Specific Instruction Set Processors is on the energy aware architecture exploration of domain specific instruction set processors and the co optimization of the datapath architecture foreground memory and instruction memory organisation with a link to the required mapping techniques or compiler steps at the early stages of the design By performing an extensive energy breakdown experiment for a complete embedded platform both energy and performance bottlenecks have been identified together with the important relations between the different components Based on this knowledge architecture extensions are proposed for all the bottlenecks

Transaction-Level Power Modeling Amr Baher Darwish, Magdy Ali El-Moursy, Mohamed Amin

Dessouky, 2019-08-01 This book describes for readers a methodology for dynamic power estimation using Transaction Level Modeling TLM The methodology exploits the existing tools for RTL simulation design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling TLPM Readers will benefit from this innovative way of evaluating power on a high level of abstraction at an early stage of the product life cycle decreasing the number of the expensive design iterations

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